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10/679,594	10/06/2003	Neil Johnson	ALT.P026	5941

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EXAMINER	
FARROKH, HASHEM	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,594	JOHNSON, NEIL	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,18,20-24,26,27,33-35 and 37-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *38-51* is/are allowed.

6)☒ Claim(s) *16,18,20-24,26,27,33-35 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The instant application having application No. 10/679,594 has a total of 37 claims pending in the application; claims 16, 23, 33, 38-39, and 47-48 have been amended; claims 1-15, 17, 19, 25, 28-32, and 36 have been canceled; no new claims have been added.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 16, 18, 20-21, 23-24, 26-27,33-35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5, 867,727 to Hattori in view of U.S. Patent No. 5,557,750 to Moore et al. (hereinafter Moore) and U.S. Patent No. 6,615,296 B2 to Daniel et al. (hereinafter Daniel).

1. *In regard to claim 16, Hattori teaches:*

"A method for managing data," **(e.g., see claim 16))** comprising:"

"selecting a first first-in-first-out (FIFO) memory from a plurality of (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device," **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.17).** *For example the address bits A7 to A5 coincide with the bits*

set in the FIFO is selected and the oldest (e.g., first data-in) data or first data is read out. However, Hattori does not expressly teach: "wherein the first data was prepared for output prior to a generation of the first read address from the data reading device; and preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device."

Moore teaches: "wherein the first data was prepared for output prior to a generation of the first read address from the data reading device;" **(e.g., see column 7, lines 66-67 to column 8, lines 1-3; Fig. 2)** *For preparing the next data for prefetching within a clock cycle.*

Daniel teaches: "preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device..." **(e.g., see column 5, lines 63-64)** *For providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the next location within the FIFO to be read.*

Disclosures by Moore, Hattori, and Daniel are analogous because all references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system taught by Hattori to include prefetching disclosed by Moore furthermore to include the read pointer taught by Daniel.

The motivation for using prefetching data as taught by column 2, lines 4-7 of the Moore is to allow data to be available within one clock cycle, eliminating host waiting for an internal data bus cycle. By thus eliminating host-waiting state, overall system performance is significantly enhanced. Furthermore, the motivation for using RP as taught by column 5, lines 62-63 of Daniel is to reduce the number of access required. This reduction would significantly increase FIFO throughput.

Therefore, it would have been obvious to combined teaching of Daniel and Moore with Hattori to obtain the invention as specified in the claim.

2. *In regard to claims 18 and 35 Moore teaches:*

"wherein the first data is output within a clock cycle after the first read address from the data reading device is generated." **(e.g., see column 7, lines 23-24; and lines 66-67 to column 8, lines 1-4; Fig. 2).**

3. *In regard to claims 20 and 26 Hattori teaches:*

"selecting a second FIFO memory from the plurality of FIFO memories to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device;" **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.15).** *Hattori teaches that first FIFO 38-1 and second FIFO 38-2 can be selected for reading by providing address bits 31 to 5 to decoding circuit 70 (e.g., see Fig. 15). Address 7 to 5 to select 1 of the 8 FIFOs 38-1 to 38-2. The control processors provide addresses A31 to A5 to decoding circuits for reading data from any of the 8 FIFOs. However, Hattori does not expressly teach:* "preparing next data from a next storage element from the second FIFO memory for output."

Moore teaches: "preparing next data from a next storage element from the second FIFO memory for output." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).**

4. *In regard to claims 21, 27, and 37 Hattori teaches:* selecting any of plurality of 8 FIFOs for data output but does not expressly teaches: "... preparing of the next data from the next storage element ..."

Moore teaches: "... preparing of the next data from the next storage element ..." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).**

5. *In regard to claim 23, Hattori teaches:*

"A method for managing data **(e.g., see claim 16)**, comprising:"

"selecting a first first-in-first-out (FIFO) memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device," **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.17).** *For example the address bits A7 to A5 coincide with the bits set in the FIFO is selected and the oldest (e.g., first data-in) data or first data is read out. However, Hattori does not expressly teach:* "wherein the first data is output within a clock cycle after the first read address is generated; and preparing next data from a next storage element from the first FIFO memory for output."

Moore teaches: "wherein the first data is output within a clock cycle after the first read address is generated;" **(column 7, lines 23-24; and lines 66-67 to column 8, lines 1-4; Fig. 2).**

Daniel teaches: "preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device..." **(e.g., see column 5, lines 63-64)** *For providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the next location within the FIFO to be read. The motivation for combining is based on the same rational given in claim 16.*

6. *In regard to claims 24 and 34 Moore teaches:*

"wherein the first data was prepared for output by the first FIFO memory prior to a generation of the read address from the data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).** *For example data is prepared and stored in prefetch register prior to next Bus cycle (e.g., prior to generation or read address).*

7. *In regard to claim 33, Hattori teaches:*

"A method for managing data **(e.g., see claim 16)**, *comprising:"*

"selecting a first first-in-first-out (FIFO) memory from a plurality of FIFO memories **(e.g., elements 38-1 to 38-8 in Fig. 12)** to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device;" **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.15).**

"selecting a second FIFO memory from the plurality of FIFO memories to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device;" **(e.g., see column 11, lines 60-**

67 to column 12, lines; Fig.15). *Hattori teaches that first FIFO 38-1 and second FIFO 38-2 can be selected for reading by providing address bits 31 to 5 to decoding circuit 70 (e.g., see Fig. 15). Address 7 to 5 to select 1 of the 8 FIFOs 38-1 to 38-2. The control processors provide addresses A31 to A5 to decoding circuits for reading data from any of the 8 FIFOs. However, Hattori does not expressly teach: "preparing next data from a next storage element from the second FIFO memory for output."*

Moore teaches: "preparing next data from a next storage element from the second FIFO memory for output..." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).** *For example preparing data to be ready in prefetch register.*

Daniel teaches: "...by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device..." **(e.g., see column 5, lines 63-64)** *for providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the next location within the FIFO to be read. The motivation for combining is based on the same rational given in claim 16.*

Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori in view of Moore and Daniel as applied to claim16 above, and further in view of U.S. Patent Publication 2002/0152263 A1 to Goldrian et al. (hereinafter Goldrian).

8. In regard to claim 22, the Hattori in view of Moore and Daniel teach all limitations recited in claim 16 but does not expressly teach: "writing data into the plurality of FIFO memories in a round robin fashion."

Goldrian teaches: "writing data into the plurality of FIFO memories in a round robin fashion." **(e.g., see paragraph 71 in page 4)** *for writing to FIFOs in a round-robin fashion.*

Disclosures by Hattori, Moore, Daniel and Goldrian are analogous because all references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system and method taught by Hattori, Moore, Daniel to include writing to FIFOs in round-robin fashion taught by Goldrian.

The motivation for using round-robin as taught by paragraph 58, page 3 of Goldrian is to keep the packet sequence in order.

Therefore, it would have been obvious to combined teaching of Goldrian, Moore, Daniel, and with Hattori to obtain the invention as specified in the claim.

Allowable Subject Matter:

Claims 38-51 are allowed

1. The primary reasons for allowance of independent claims 38-51 in the instant application is the combination with the inclusion of following limitations: **a memory read manager to tie assert read enable inputs of the FIFO memories and to select a**

in the first FIFO memory in response to a first read address from a data reading device.

Response to Applicant Remarks

The Applicant argument in regard to the amended independent claims 38 and 48 is persuasive. In regard to rejections of the independent claims 16, 23, and 33 Applicant make a general allegation without specifically pointing out why the references do not teach the limitations recited in the claims. For example in page 18 to page 19 of his Remarks Applicant state:

"In contrast, claim 16 states
A method for managing data, comprising:
selecting a first first-in-first-out (FIFO.) memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory, in response to a first read address from a data reading device, wherein the first data was prepared for output prior to generation of the first read address from the data reading device; and preparing next data from a next storage element from the first FIFO memo for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.
(Claim 16) (Emphasis Added).
Claims 23, 38, and 47 include similar limitations. Claim 33 includes the limitation regarding preparing next data. Given that claims 18, and 20-22 depend from claim 16, claims 24, 26, and 27 depend from claim 23, claims 34-35, and 37 depend from claim 33, and claims 39-46 depend from claim 38, and claims 48-51 depend from claim 47, it is likewise submitted that
claims 18, 20-22, 24, 26, 27, 34-35, 37, 39-46, and 48-51 arc also patentable under 35 U.S.C. § 102(e) and § 103(a) over Karnstedt, Hattori, Moore, Daniel, Goldrain, Daniel, and Brebner."

Since claims 38-51 are now considered allowable, arguments regarding these claims are moot. However, in regard to rejection of claims 16, 18, 20-24, 26-27, 33-35, and 37 the Examiner believes that combination Hattori, Moore, Daniel, and Goldrian

teaches all limitations included in the claims. Accordingly, in regard to rejection of claims 16, 18, 20-24, 26-27, 33-35, and 37 the Examiner maintains his position.

Conclusion

THIS ACTION IS MADE FINAL. *Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information

for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

HF

2007-05-27

Brian R. Peugh
Primary Examiner
5/28/07